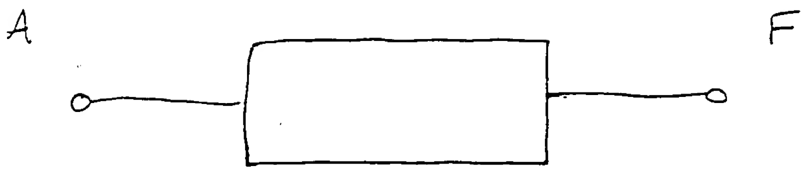

FIG 1.

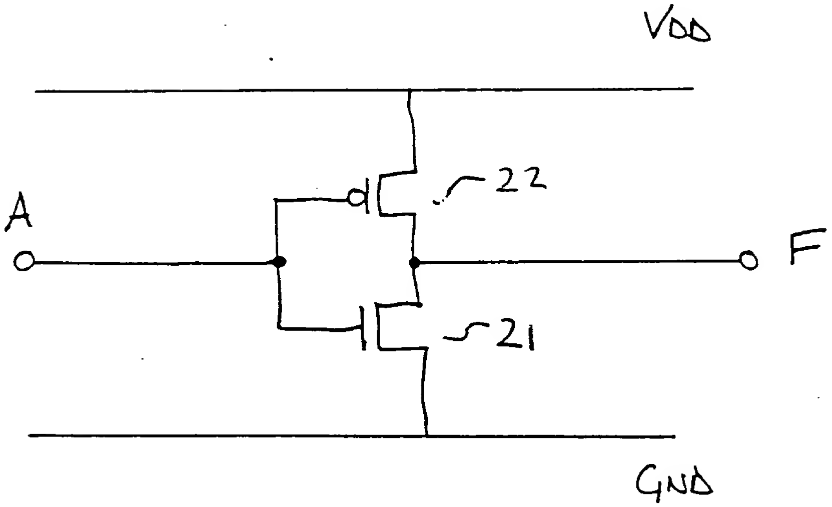

FIG 2.

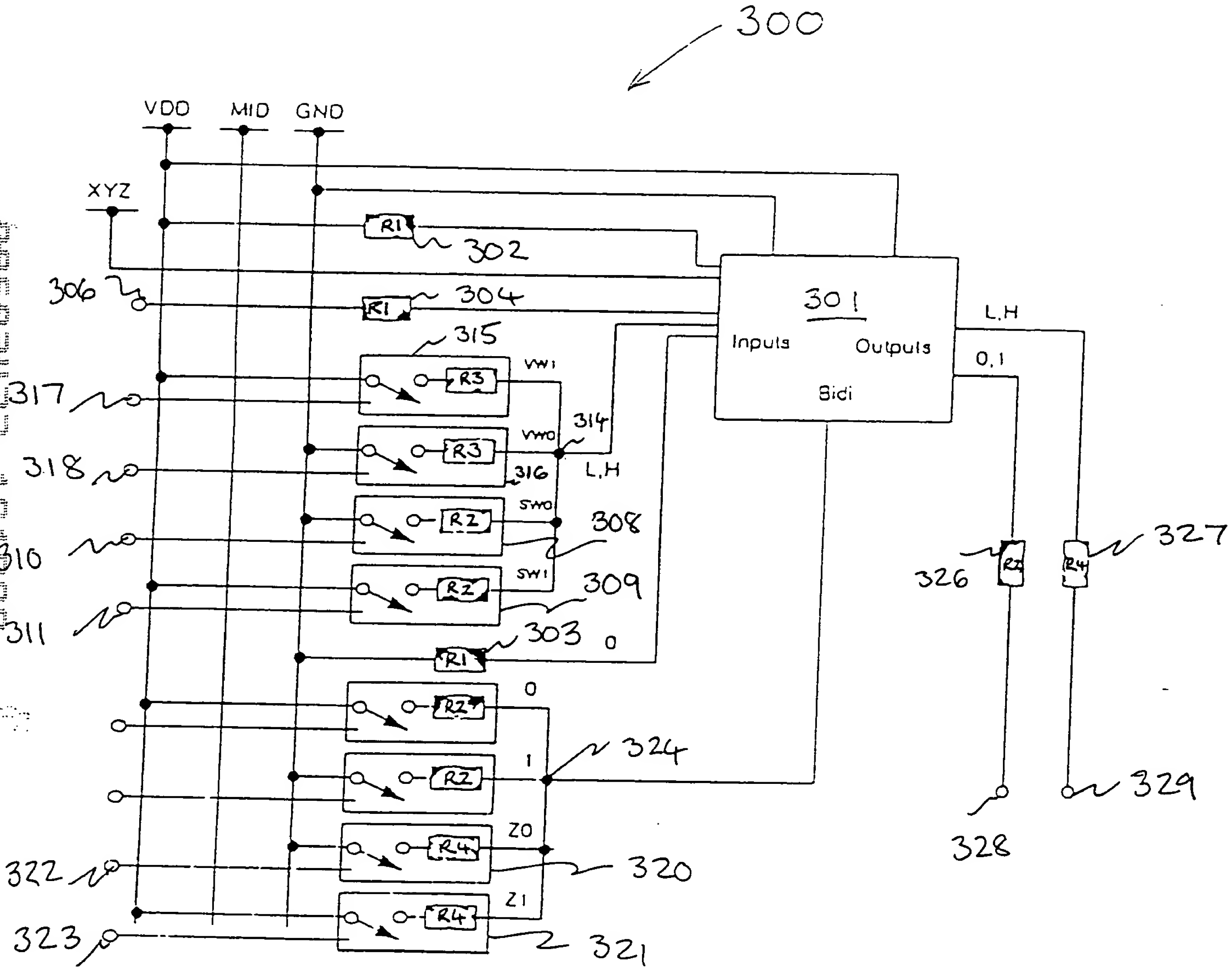
300
VDD
MID
GND
XYZ
R1
302
306
R1
304
301
Inputs
Outputs
Bidi
L,H
0,1
315
R3
VW1
317
R3
VW0
314
L,H
318
316
R2
SW0
308
310
R2
SW1
309
311
R1
303
0
R2
0
324
R2
1
R4
Z0
322
320
R4
Z1
323
321
R2
R4
326
327
328
329

FIG 3.

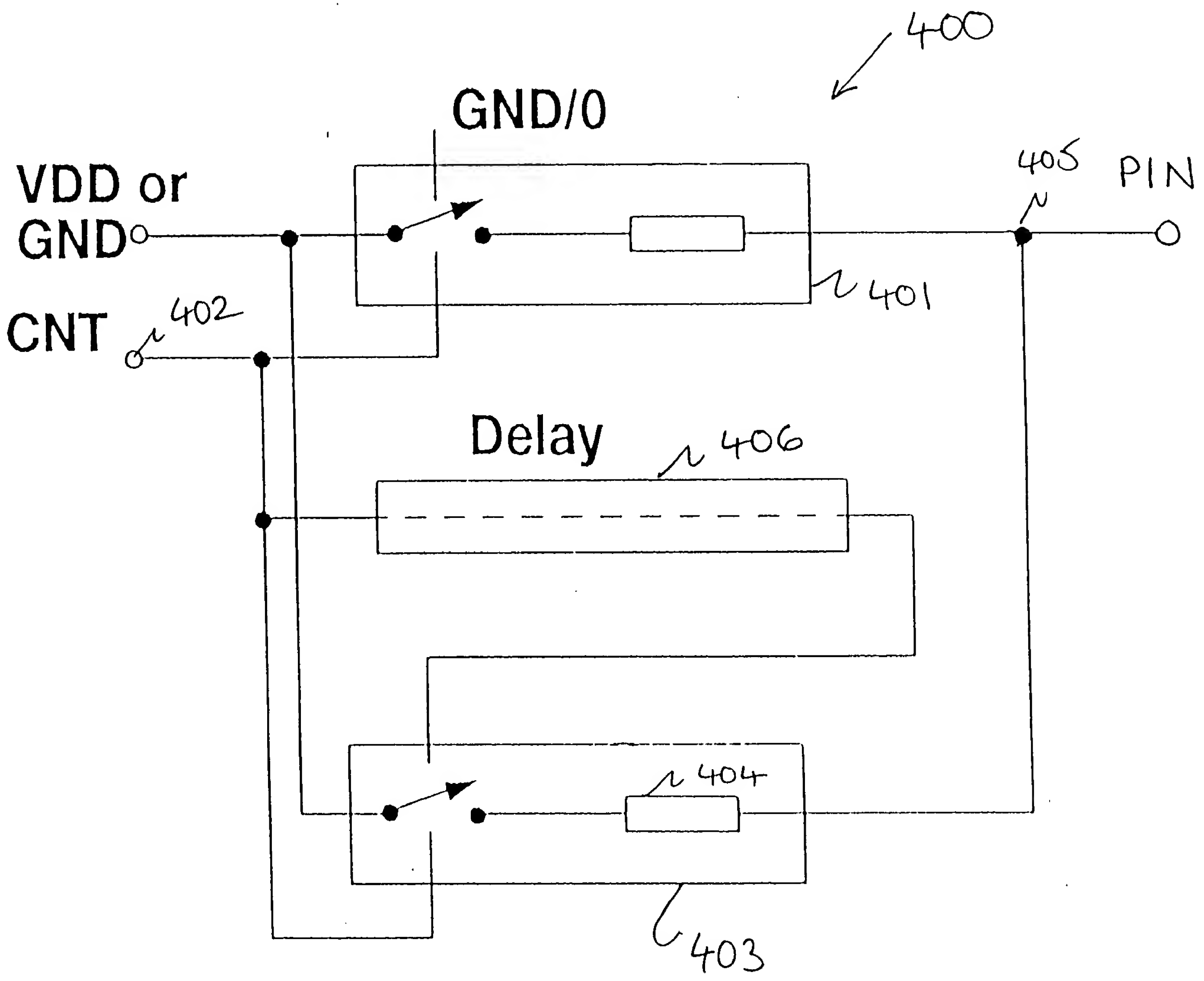

FIG 4.

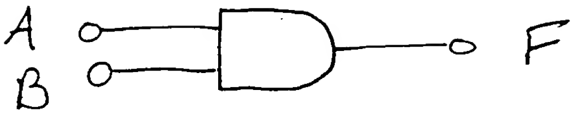

FIG 5.

URE 6

```
WIF2TB Flow Diagram
===================

      /------------\
      |   Start    |- S1
      \------------/
            |

Stage  0 ----- Binary represntation = 000000 ------------- Stage  0

            |
      /------------\~S2
      | Read   WIF | DBmain = WIF data
      \------------/
            |

Stage  1 ----- Binary represntation = 000001 ------------- Stage  1

            |
     /-------------\ ~S3
     | Weaken BIDs | 0 = L, 1 = H, X = W
     \-------------/
            |

Stage  2 ----- Binary represntation = 000010 ------------- Stage  2

            |
  /--------------------\~S4
  | Write out VHDL TB  | VHDL = DBmain
  | Write control file | Tracing = none
  \--------------------/ Model in WORK cellname_pack
            |
            |
    /-----------------\~S5
    | Analyse VHDL TB | VSS = VHDL
    \-----------------/
            |
            |
  /-------------------\~S6
  |   Simulate VHDL   | OW +? REAL = VSS
  |  Convert Results  | WIFhdl = OW +? REAL
  | Check Assertions  | Stop if errors/known assertions
  \-------------------/
            |
            |
      /------------\ ~S7
      | Read   WIF | DBslave = WIF data
      \------------/
            |
            |                   S8
  /-------------------\
  | Copy O/P patterns | DBmain(o/p) = DBslave(o/p)
  \-------------------/
            |
            |
   /-----------------\-S9
   | Expand Level Xs | X = OM1 ?
   \-----------------/
            |
Stage  4 ----- Binary represntation = 000100 ------------- Stage  4

                 |
      /-----------------\~510
      | Expand  Edge Xs | X = 0M1 ?
      \-----------------/
                 |

Stage  8 ----- Binary represntation = 001000 ------------- Stage  8

                 |
      /-----------------\~511
      | Expand DEdge Xs | X = 0M1 ?
      \-----------------/
                 |

Stage 16 ----- Binary represntation = 010000 ------------- Stage 16

                 |
     /-------------------\~512
     | Write out VHDL TB  | VHDL = DBmain + assertions
     | Write control file | Tracing = none
     \-------------------/ Model in WORK cellname_pack
                 |
                 |
      /----------------\~513
      | Analyse VHDL TB | VSS = VHDL
      \----------------/
                 |
                 |
     /-----------------\~514
     |  Simulate VHDL   | OW +? REAL = VSS
     | ~~Convert Results~~ | WIFhdl = OW +? REAL
     | Check Assertions | Stop if errors/known assertions
     \-----------------/
                 |
                 |
     /-----------------\~515
     | Expand Output Zs | Z = Zlow, Zhigh
     \-----------------/
                 |

Stage 32 ----- Binary represntation = 100000 ------------- Stage 32

                 |
   /---------------------\~516
   | Write out ELDO file |
   \---------------------/
                 |
                 |
     /-----------------\~517
     |  Simulate ELDO   | CHI = ELDO
     | Convert Results  | WIFeldo = CHI
     \-----------------/
                 |
                 |
       /-----------\~518
       | Read  WIF | DBslave = WIF data
       \-----------/
```

```
                    |
  /-------------------\~519
  |    Verify ELDO    |  DBmain =?= DBslave
  |      Results      |  for o/p using ELDO verifier
  \-------------------/
                    |
      /------------\~520
      |  The End   |
      \------------/
```